LISTING OF THE CLAIMS:

Claim 1 (Amended) A method for fabricating a heterojunction bipolar transistor comprising ~~the steps of~~:

providing an SOI ~~structure having~~ substrate comprising a bottom Si-containing layer, a buried insulating layer located atop the bottom Si-containing layer, a top Si-containing layer atop the buried insulating layer and a sub-collector which is formed in an upper surface of the bottom Si-containing layer, said sub-collector is in direct contact with a bottom surface of the buried insulating layer;

selectively removing portions of the top Si-containing layer and the buried insulating layer stopping atop the sub-collector so to define an area for fabricating a heterojunction bipolar transistor; and

forming an extrinsic base heterojunction bipolar transistor in said area in which a base region of the transistor is formed directly atop the sub-collector.

Claim 2 (Currently Amended) The method of Claim 1 wherein the sub-collector is formed by ion implanting a dopant into said SOI ~~structure~~ substrate.

Claim 3 (Currently Amended) The method of Claim 1 wherein the sub-collector is formed during said fabrication of an SOI ~~structure~~ substrate.

Claim 4 (Currently Amended) The method of Claim 1 further comprising forming a region in said SOI ~~structure~~ substrate that is in contact with the sub-collector.

Claim 5 (Currently Amended) The method of Claim 1 further comprising forming trench isolation regions in said SOI ~~structure~~ substrate prior to said selectively removing step.

Claim 6 (Original) The method of Claim 5 wherein said trench isolation regions are selected from deep trench isolation regions, shallow trench isolation regions and a combination thereof.

Claim 7 (Original) The method of Claim 1 wherein the selectively removing step comprises a first etching process that is highly selective in removing silicon as compared to an insulator and a second etching process that is highly selective in removing an insulator as compared to silicon.

Claim 8 (Original) The method of Claim 1 wherein the base region of the bipolar transistor is formed by a low-temperature epitaxial growth process.

Claim 9 (Original) The method of Claim 8 wherein said base region includes polycrystalline portions and monocrysytalline portions.

Claim 10 (Original) The method of Claim 1 wherein the forming of the extrinsic base heterojunction bipolar transistor comprises a self-aligned process or a non-self aligned process.

Claim 11 (Original) The method of Claim 1 wherein the forming of said extrinsic base heterojunction bipolar transistor comprises the steps of: forming an extrinsic base atop said base region; forming a patterned emitter isolation oxide atop portions of said extrinsic base; forming an emitter polysilicon in an emitter opening located in the extrinsic base; and patterning the emitter polysilicon.

Claim 12 (Currently Amended) The method of Claim 1 further comprising subjecting portions of the SOI ~~structure~~ substrate that lay to the periphery of the extrinsic base heterojunction bipolar transistor to a proton ion implantation step, which increases resistivity of the SOI ~~structure~~ substrate.

Claim 13 (Original) The method of Claim 12 further comprising forming an inductor over said region of increased resistivity.

Claim 14 (Currently Amended) A BiCMOS structure comprising:

an SOI ~~structure~~ substrate having a bottom Si-containing layer, a buried insulating layer located atop the bottom Si-containing layer, a top Si-containing layer atop the buried insulating layer and a sub-collector which is located in an upper surface of the bottom Si-containing layer, said sub-collector is in contact with or close to a bottom surface of the buried insulating layer; and

an extrinsic base heterojunction bipolar transistor located in an opening provided in a bipolar device area of the SOI substrate in which a base region of the bipolar transistor is located directly atop the sub-collector.

Claim 15 (Currently Amended) The BiCMOS structure of Claim 14 further comprising at least one field effect transistor located adjacent to, but isolated from, the extrinsic base heterojunction bipolar transistor, said at least one field effect transistor is located within and atop the top Si-containing layer of the SOI ~~structure~~ substrate.

Claim 16 (Currently Amended) The BiCMOS structure of Claim 14 further comprising at least one passive element located adjacent to, but isolated from, the extrinsic base heterojunction bipolar transistor, said at least one passive element is located atop areas of the SOI ~~structure~~ substrate having increased resistivity.

Claim 17 (Original) The BiCMOS structure of Claim 14 wherein the base region is comprised of a polycrystalline portion and a monocrystalline portion.

Claim 18 (Original) The BiCMOS structure of Claim 14 wherein the extrinsic base heterojunction bipolar transistor includes an extrinsic base that is comprised of a doped layer.

Claim 19 (Original) The BiCMOS structure of Claim 14 wherein the extrinsic base heterojunction bipolar transistor includes an emitter polysilicon.

Claim 20 (Currently Amended) A method for fabricating a heterojunction bipolar transistor comprising ~~the steps of~~:

providing an SOI ~~structure~~ substrate having a bottom Si-containing layer, a buried insulating layer located atop said bottom Si-containing layer, a top Si-containing layer atop said buried insulating layer and a sub-collector which is formed in an upper surface of said bottom Si-containing layer, said sub-collector is in direct contact with a bottom surface of the buried insulating layer;

selectively removing the top Si-containing layer from a portion of said SOI ~~structure~~ substrate to provide a bipolar opening;

depositing a bipolar dielectric within said bipolar opening, wherein said bipolar dielectric is positioned atop said buried insulating layer;

selectively removing portions of said bipolar dielectric and said buried insulating layer stopping atop said sub-collector so to define an area for fabricating a heterojunction bipolar transistor; and

forming an extrinsic base heterojunction bipolar transistor in said area in which a base region of the transistor is formed directly atop the sub-collector.

Claim 21 (Currently Amended) The method of Claim 20 wherein said sub-collector is formed by ion implanting a dopant into said SOI ~~structure~~ substrate.

Claim 22 (Currently Amended) The method of Claim 20 wherein the sub-collector is formed during the fabrication of an SOI ~~structure~~ substrate.

Claim 23 (Original) The method of Claim 20 wherein following said selectively removing portions of said bipolar dielectric and said buried insulating layer, a conformal oxide liner is grown within said area for fabricating said heterojunction bipolar transistor.

Claim 24 (Original) The method of Claim 23 further comprising forming at least one set of sidewall spacers atop said conformal oxide liner prior to forming said base region.

Claim 25 (Original) The method of Claim 24 further comprising removing said conformal oxide liner from a top surface of said bottom Si-containing layer, wherein said removing said conformal oxide liner comprises etching said conformal oxide liner selective to said bottom Si-containing layer.

Claim 26 (Original) The method of Claim 20 further comprising forming an n-type epitaxial silicon-containing layer atop said lower Si-containing layer within said area for fabricating said heterojunction bipolar transistor prior to forming said base region.

Claim 27 (Original) The method of Claim 20 wherein the forming of the extrinsic base heterojunction bipolar transistor comprises the steps of: forming an extrinsic base atop the base region; forming a patterned emitter isolation oxide atop portions of the extrinsic base; forming an emitter polysilicon in an emitter opening located in the extrinsic base; and patterning the emitter polysilicon.

Claim 28 (Original) The method of Claim 20 further comprising subjecting portions of the SOI substrate that lay to the periphery of the extrinsic base heterojunction bipolar transistor to a proton ion implantation step, which increases resistivity of the SOI substrate.

Claim 29 (Original) The method of Claim 28 further comprising forming an inductor over said region of increased resistivity.